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APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/654,776	09/05/2000	Chia-Ta Hsieh	TSMC98-231B	9675

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EXAMINER
LOKE, STEVEN HO YIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/654,776	HSIEH ET AL.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *29 and 33-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *29 and 33-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *02 December 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. Claim 35 is objected to because of the following informalities: Claim 35, line 3, the phrase "1000 to 3000" is unclear as to what is the unit of the thickness of the second conductive layer. Appropriate correction is required.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claim 29 is rejected under 35 U.S.C. 102(e) as being clearly anticipated by Doan (U.S. patent no. 6,271,561).

In regards to claim 29, Doan shows all the elements of the claimed invention in figs. 1A-8. It is a stacked-gate flash memory having a shallow trench isolation with a high-step oxide [26], comprising: a substrate [10] having a gate oxide layer [38]; at least two trenches [20] formed to a depth of less than about 1 micron below the surface of the substrate; an oxide layer [24] formed over the substrate, including over the inside walls of the two trenches; a high-step oxide [26] formed within the two trenches over the oxide

layer [24] and protruding upward over the surface of the substrate to a height of 3000 angstroms; the high-step oxide [26] forming an opening with high walls over the surface of the substrate between the two trenches; a first conductive layer [36A] formed conformally inside the opening and over the surface of the substrate between the high walls to form a floating gate having folding surfaces; an intergate oxide layer [42] formed over the floating gate [36A] having folding surfaces; a second conductive layer [44] formed protruding downward in between the folding surfaces over the intergate oxide layer [42] to form a control gate.

Since the source line [14] is parallel to the trench [20], it is inherent that the source line [14] is a self-aligned source line.

Since the floating gate has folding surfaces, it is inherent that there is high lateral coupling between the floating gate and the control gate.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doan (U.S. patent no. 6,271,561).

In regards to claim 33, Doan differs from the claimed invention by not showing the opening has a width between about 1500 to 5000 angstroms. It would have been obvious for the opening has a width between about 1500 to 5000 angstroms, since it has been held that where the general conditions of a claim are disclosed in the prior art,

discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

In regards to claim 34, Doan further discloses the first conductive layer [36A] is polysilicon. Doan differs from the claimed invention by not showing the first conductive layer having a thickness between about 100 to 500 angstroms It would have been obvious for the first conductive layer having a thickness between about 100 to 500 angstroms, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

In regards to claim 35, Doan further discloses the second conductive layer [44] is polysilicon. Doan differs from the claimed invention by not showing the second conductive layer having a thickness between about 1000 to 3000 angstroms It would have been obvious for the second conductive layer having a thickness between about 1000 to 3000 angstroms, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

6. Applicant's arguments filed 12/2/02 have been fully considered but they are not persuasive.

It is urged, in page 6 of the remarks, that Doan never discloses anywhere "a floating gate having folding surfaces". It is also urged that the first conductive layer 36A which becomes floating gate 50, has flat bottom and top surfaces without any folded surfaces of the invention. In addition, the first conductive layer 36A is planarized flat using

chemical mechanically polishing to form floating gates. However, as shown in figs. 1E, 1F, 4, 5 and col. 6, lines 9-29 of the specification, the first conductive layer 36 of fig. 1E can be planarized to an endpoint 40 of the trench isolation structures 30 to form a planarized first conductive layer 36A. Fig. 4 further discloses the first conductive layer 36A substantially covers the recesses 34. Therefore, the drawings and the written description show the planarized first conductive layer 36A comprises a flat bottom portion formed on the gate oxide [38] and the sidewall portions formed adjacent to the sidewalls of the oxide layers [26]. The first conductive layer 36A is then patterned and etched to form the floating gate electrode [50] (fig. 5). Doan does show a floating gate [50] having folding surfaces. Since fig. 5A is a cross section view of the floating and control gates parallel to the bit lines (fig. 5), fig. 5A shows only the flat bottom and top surfaces of the floating gate [50]. When the cross section of fig. 5 is along a direction perpendicular to the bit lines, fig. 5 also discloses the floating gate [50], the intergate oxide layer [42] and the control gate [48] having folding surfaces (fig. 1G). It is believed that Doan meets the claimed limitation of claim 29.

It is urged, in pages 6 and 7 of the remarks, that Doan does not disclose the several-fold coupling area between the floating gate and the control gate due to the higher and several folding interior walls of the floating gate formed against the high-step oxide protruding over the shallow trench isolation. However, Doan discloses the several-fold coupling area between the floating gate [36A] and the control gate [44] due to the higher and several folding interior walls of the floating gate formed against the high-step oxide [26] protruding over the shallow trench isolation [30] (figs. 1G and 5).

It is urged, in pages 7 and 8 of the remarks, that Doan never discloses anywhere "a floating gate having folding surfaces". However, as mentioned in the rejection and the above explanation to the remarks, Doan does disclose a floating gate [36A] having folding surfaces to increase several-fold the coupling between the floating gate and the control gate. In addition, fig. 1G of Doan also shows the intergate oxide layer [42] and the control gate [44] having folding surfaces. Fig. 1G shows the floating gate [36A], the intergate oxide layer [42] and the control gate [44] overlay each other conformally. It is believed that claims 33-35 are obvious over Doan for the reasons given above.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

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February 19, 2003

Steven Loke